IN THE CLAIMS:

Please cancel claim 3 without prejudice or disclaimer, amend claims 2 and 4-7, and add new claims 8-9 as follows:

1. (Cancelled)

2. (Currently Amended) A logic verification system comprising:

a logic simulation accelerator including:

a logic simulator operating on a general purpose processor to logically verify operation correctness of a designed logic circuit;

a device ~~including~~ which includes a programmable [[EPGA]]FPGA module composed by FPGAs to be programmed to physically realize functions of the designed logic circuit and which is mounted to the logic simulator via a connector; and

a bridge circuit which is mounted to the logic simulator and which selectively transmits and receives corresponding data between ~~said logic simulator operating on said general purpose processor and said FPGA module according to designed functions assigned to said EPGAs for each of a plurality of designed logic circuits~~ said general purpose processor and said device,

wherein all pins of the FPGA module ~~used in a verification process for verifying one of said plurality of designed logic circuits by said logic simulator~~ are wired ~~in direct~~ directly to the bridge circuit via the connector ~~to accelerate logic simulation~~,

wherein a cutting end of a verification logic ~~of said one of the plurality of~~ which verifies said designed logic circuit[[s]] realized on said device is assigned to ~~an external interface~~ the connector of the FPGA module for accelerating logic simulation, and

wherein a correspondence between each ~~pin of the external interface connector~~ of said all pins of said FPGA module and a logic signal from said general purpose processor is established on said logic simulator ~~on said general purpose processor~~, and

wherein the verification logic for verifying said designed logic circuit implemented on said device provides a means for transmitting a direction control

signal which controls a transmission direction of two-way signals between said FPGA module and said bridge circuit thereby performing logic verification of the designed logic circuit by the logic simulator in parallel with physical realization of the designed logic circuit one said device, and said direction control signal is sent to the bridge circuit via one of said two-way signals.

3. (Cancelled)

4. (Currently Amended) The logic verification system according to claim 2, further comprising a means for automatically detecting a signal direction of a two-way signal between said FPGA module and the bridge circuit, and program data of the same FPGA module implementing different verification logics is used in verification processes consisting of acceleration of logic simulation and logic emulation for [[the]] a plurality of designed logic circuits.

5. (Currently Amended) The logic verification system according to claim 4, wherein said means for automatically detecting the signal direction of the two-way signal sets a drivability level of output circuits of the [[EPGA]]FPGA module and the bridge circuit, and ~~giving a~~ gives priority in determination of signal direction to one of the [[EPGA]]FPGA module and the bridge circuit ~~having~~ which has a higher drivability.

6. (Currently Amended) The logic verification system according to claim 4, further comprising: a means for inputting the signal direction of the two-way signal to the logic simulator on the general purpose processor,

wherein a disagreement between [[a]] the signal direction of the two-way signal to the logic simulator and a signal direction indicted in said direction control signal ~~of the FPGA module~~ is detected by comparing said signal directions.

7. (Currently Amended) The logic verification system according to claim 6, wherein said means for automatically detecting the signal direction of the two-way signal sets a drivability level of output circuits of the [[EPGA]]FPGA module and the bridge circuit, and ~~giving the~~ gives priority in determination of signal direction to one of the [[EPGA]]FPGA module and the bridge circuit ~~having~~ which has a higher drivability.

8. (New) The logic verification system according to claim 2, wherein said direction control signal is added into the verification logic.

9. (New) The logic verification system according to claim 2, wherein said direction control signal is instead transmitted on a time division basis with said two-way signals.